Amendments to the Claims:

1. (currently amended) A semiconductor wafer comprising:

a substrate;

a plurality of integrated circuits chips fabricated on said substrate;

a dicing channel disposed between adjacent ones of said integrated circuits chips, said channel exposing sidewalls of said integrated circuits;

a layer of first dielectric material disposed on a top surface and sidewalls of said integrated circuits chips; and

at least one layer of at least one second dielectric material disposed on said layer of first dielectric material, wherein said first dielectric material has a G_c value of at least about 10 times greater than said second dielectric material.

2. (original) The semiconductor wafer of Claim 1, wherein said first dielectric material has a G_c value greater than about 0.1 kJ/m^2.

3. (original) The semiconductor wafer of Claim 1, wherein said first dielectric material has a G_c value of about 0.5 to about 2.5 kJ/m^2.

4. (original) The semiconductor wafer of Claim 1, wherein said second dielectric material has a G_c value less than about 0.05 kJ/m^2.

5. (original) The semiconductor wafer of Claim 1, wherein said second dielectric material has a G_c value of about 0.005 to about 0.05 kJ/m^2.

6. (original) The semiconductor wafer of Claim 1, wherein said first dielectric material has a tensile strength of about 20 to 100 MPa.

7. (original) The semiconductor wafer of Claim 1, wherein said second dielectric material has a tensile strength of about 700 to 10,000 MPa.

8. (original) The semiconductor wafer of Claim 1, wherein said first dielectric material is selected from the group consisting of polyesters, phenolics, polyimides, polysulfones, polyether ether ketones, polyurethanes, epoxies, polyarylene ethers, and polyethylene terepthalates.

9. (original) The semiconductor wafer of Claim 1, wherein said first dielectric material is a polyarylene ether.

10. (original) The semiconductor wafer of Claim 1, wherein said second dielectric material is selected from the group consisting of SiN_x, SiO_2, SiC, TEOS, FTEOS, FSG, and OSG.

11. (original) The semiconductor wafer of Claim 1, wherein said second dielectric material is SiO_2.

12. (currently amended) The semiconductor wafer of Claim 1, wherein said dicing channel exposes sidewalls of said integrated circuits chips and sidewalls of said substrate.

13. (currently amended) The semiconductor wafer of Claim 1, further comprising a plurality of conductors embedded in said first dielectric material and said second dielectric material and in contact with said plurality of integrated circuits chips.

14. (currently amended) The semiconductor wafer of Claim 13, wherein said conductors are ~~S-shaped or spring shaped or~~ jogged.

15. (original) The semiconductor wafer of Claim 1, wherein said semiconductor wafer comprises a plurality of layers of said at least one second dielectric material.

16. (original) The semiconductor wafer of Claim 15, wherein at least one of said layers of second dielectric material is SiO_2, and at least one of said layers of second dielectric material is SiN_x.

17-31. (withdrawn)